Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-13 (Cancelled)

Claim 14. (Original) An integrated circuit comprising:

a series of circuits;

a phase detector having a first input coupled to an input of the series of circuits and a second input coupled to an output of the series of circuits;

an up/down counter having an input coupled to an output of the phase detector; and

a first variable-delay block having a control input coupled to an output of the up/down counter,

wherein the series of circuits comprises:

a second variable-delay block having a control input coupled to the output of the up/down counter; and

a frequency divider.

Claim 15. (Original) The integrated circuit of claim 14 further comprising:

a first register having an input coupled to an output of the input buffer and a clock input coupled to an output of the first variable-delay block; and

a second register having an input coupled to the output of the input buffer and a complementary clock input coupled to the output of the first variable-delay block.

Claim 16. (Original) The integrated circuit of claim 15 further comprising:

a third flip-flop coupled between the phase detector and the up/down counter.

Claim 17. (Original) The integrated circuit of claim 14 wherein an input of the second variable-delay block is coupled to an output of the frequency divider.

Claim 18. (Original) The integrated circuit of claim 14 wherein an output of the frequency divider is coupled to an input of the second variable-delay block.

Claim 19. (Original) An integrated circuit comprising:

a series combination of a first frequency divider and a first variable-delay block, configured to receive a first clock signal;

a phase detector configured to receive the first clock signal and an output from the series combination;

an up/down counter configured to receive an output from the phase detector; and

a second variable-delay block configured to receive a second clock signal,

wherein the first variable-delay block and the second variable-delay block are configured to receive an output from the up/down counter.

Claim 20. (Original) The integrated circuit of claim 19 wherein the first frequency divider is configured to receive the first clock signal and the first variable-delay block is configured to receive an output from the first frequency divider.

Claim 21. (Original) The integrated circuit of claim 19 wherein the first variable-delay block is configured to receive the first clock signal and the first frequency divider is configured to receive an output from the first variable-delay block.

Claim 22. (Currently amended) The integrated circuit of claim 19 further comprising:

a first flip-flop having a clock input configured to receive an output of the ~~first~~ second variable-delay block; and

a second flip-flop having a complementary clock input configured to receive the output of the ~~first~~ second variable-delay block.

Claim 23. (Original) The integrated circuit of claim 22 further comprising:

a memory configured to receive an output of the first flip-flop and an output of the second flip-flop.

Claim 24. (Original) The integrated circuit of claim 22 further comprising:

an synchronous dynamic random access memory configured to receive an output of the first flip-flop and an output of the second flip-flop.

Claim 25. (Currently amended) The integrated circuit of claim ~~19~~ 22 further comprising:

a third flip-flop coupled between the phase detector and the up/down counter.

Claim 26. (Original) The integrated circuit of claim 25 further comprising:

a second frequency divider configured to receive the first clock signal to provide a third clock signal to the up/down counter.

Claim 27. (Original) The integrated circuit of claim 19 wherein the integrated circuit is a programmable logic device.

Claim 28. (Original) A computing system comprising:

a multiple-data-rate memory; and

the integrated circuit of claim 14 coupled to the multiple-data-rate memory.

Claim 29. (Original) The computing system of claim 28 wherein the multiple-data-rate memory is a double-data-rate memory.

Claim 30. (Original) An integrated circuit comprising:

a series of circuits comprising:

a dividing means for dividing a frequency of a clock signal; and

a first delaying means for delaying a clock signal by a first duration,

wherein the series of circuits receives a first clock signal and provides a second clock signal, the second clock signal delayed and divided in frequency from the first clock signal;

phase detector means for receiving the first and second clock signals, and providing an output;

a second delaying means for delaying a third clock signal by a second duration; and

adjustment means for increasing or decreasing the first and second durations based on the output of the phase detector means.

Claim 31. (Original) The integrated circuit of claim 30 wherein the series of circuits provides the second clock signal by first dividing the frequency of the first clock signal.

Claim 32. (Original) The integrated circuit of claim 31 wherein the frequency of the first clock signal is divided by a value selected from the group consisting of 4, 8, and 16.

Claim 33. (Original) The integrated circuit of claim 30 wherein the series of circuits provides the second clock signal by delaying the first clock signal before dividing its frequency.

Claim 34. (New) An integrated circuit comprising:

a first input buffer having an input coupled to a first pad;

a double data rate register comprising:

a first register having a data input responsive to a signal at an output of the first input buffer and a rising-edge triggered clock input; and

a second register having a data input coupled to the data input of the first register and a falling-edge triggered clock input coupled to the rising-edge triggered clock input of the first register; and

a delay circuit comprising:

an up/down counter; and

a variable delay block coupled to provide a delay between a signal at the data input of the first register and a signal at the rising-edge triggered clock input of the first register.

Claim 35. (New) The integrated circuit of claim 34 wherein a count provided by the up/down counter sets the delay between the signal at the data input of the first register and the signal at the rising-edge triggered clock input of the first register.

Claim 36. (New) The integrated circuit of claim 35 further comprising a bypass path to bypass the variable delay element.

Claim 37. (New) The integrated circuit of claim 35 further comprising a multiplexer having a first input coupled to an input of the variable delay element and an output coupled to an output of the variable delay element.

Claim 38. (New) The integrated circuit of claim 35 further comprising:

a second input buffer coupled to a second pad to receive a DQS signal,

wherein the rising-edge triggered clock input of the first register is responsive to a signal at the output of the second input buffer, and a DQ signal is received at the first pad.

Claim 39. (New) The integrated circuit of claim 38 wherein a clock signal is used in generating the count provided by the up/down counter.

Claim 40. (New) The integrated circuit of claim 35 further comprising:

a plurality of programmable logic elements, configurable to perform user-defined logic functions; and

a plurality of logic interconnect lines configurable to couple the plurality of programmable logic elements to the double-data rate register.

Claim 41. (New) The integrated circuit of claim 35 wherein the variable delay block comprises a series of delay elements.

Claim 42. (New) An integrated circuit comprising:

a first input buffer having an input coupled to a first pad;

a first register having a data input responsive to a signal at an output of the first input buffer and a rising-edge triggered clock input;

a second register having a data input coupled to the data input of the first register and a falling-edge triggered clock input coupled to the rising-edge triggered clock input of the first register; and

a delay circuit comprising:

a control circuit including an up/down counter;

a variable delay circuit coupled to provide a variable delay between a signal at the data input of the first register and a signal at the rising-edge triggered clock input of the first register; and

a multiplexer having a first input coupled to an input of the delay circuit and a second input coupled to an output of the delay circuit.

Claim 43. (New) The integrated circuit of claim 42 the up/down counter provides a count to the delay circuit,

wherein the count determines the delay between the signal at the data input of the first register and the signal at the rising-edge triggered clock input of the first register.

Claim 44. (New) The integrated circuit of claim 43 wherein the multiplexer provides a bypass path for bypassing the delay circuit.

Claim 45. (New) The integrated circuit of claim 43 further comprising:

a second input buffer coupled to a second pad to receive a DQS signal,

wherein the rising-edge triggered clock input of the first register is responsive to a signal at the output of the second input buffer, and a DQ signal is received at the first pad.

Claim 46. (New) The integrated circuit of claim 45 wherein a clock signal is used in generating the count provided by the up/down counter.

Claim 47. (New) The integrated circuit of claim 43 further comprising:

a plurality of programmable logic elements, configurable to perform user-defined logic functions; and

a plurality of logic interconnect lines configurable to couple the plurality of programmable logic elements to the first register and the second register.

Claim 48. (New) The integrated circuit of claim 43 wherein the integrated circuit is a field programmable gate array.

Claim 49. (New) The integrated circuit of claim 43 wherein the variable delay circuit comprises a series of delay elements.

Claim 50. (New) An integrated circuit comprising:

a rising-edge triggered register having a data input and a clock input;

a falling-edge triggered register having a data input coupled to the data input of the rising-edge triggered register and a clock input coupled to the clock input of the rising-edge triggered register;

a series of delay circuits coupled to provide a variable delay between a signal at the data input and a signal at the clock input of the first register;

a multiplexer having an input coupled to an input of the series of delay circuits and an output coupled to an output of the series of delay circuits; and

a counter having an output coupled to series of delay circuits.

Claim 51. (New) The integrated circuit of claim 50 wherein the counter provides a count to the series of delay circuits;

wherein the count is incremented and decremented to vary the variable delay.

Claim 52. (New) The integrated circuit of claim 50 wherein the multiplexer provides a bypass path for bypassing the series of delay circuits.

Claim 53. (New) The integrated circuit of claim 50 further comprising:

a second input buffer coupled to a second pad to receive a DQS signal,

wherein the clock input of the rising-edge triggered register is responsive to a signal at the output of the second input buffer, and a DQ signal is received at the first pad.

Claim 54. (New) The integrated circuit of claim 50 wherein a clock signal is used in generating the count provided by the counter.

Claim 55. (New) The integrated circuit of claim 50 further comprising:

a plurality of programmable logic elements, configurable to perform user-defined logic functions; and

a plurality of logic interconnect lines configurable to couple the plurality of programmable logic elements to the rising-edge triggered register and the falling edge-triggered register.

Claim 56. (New) The integrated circuit of claim 50 wherein an output of the rising-edge triggered register is coupled to a first-in-first-out memory.